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R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

SUPPORT FOR AMENDMENT TO THE SPECIFICATION

Support for the amendment to the specification can be found in the drawings as originally filed, for example, on FIG. 1 and in the specification as originally filed, for example, on page 2, lines 16-18. As such, no new matter has been added.

SUPPORT FOR CLAIM AMENDMENTS

Support for the amendments to the claims can be found in the drawings as originally filed, for example, on FIGS. 1-5 and in the specification as originally filed, for example, on page 1, lines 18-20, page 5, line 11 through page 6, line 15, and page 9, line 1 through page 12, line 7. As such, no new matter has been added.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1-3, 5-10 and 20 under 35 U.S.C. §102(b) as being anticipated by "IEEE Standard Test Access Port and Boundary-Scan Architecture, IEEE Std 1149.1-1990" (hereinafter IEEE Std 1149.1-1990) has been obviated by appropriate amendment and should be withdrawn.

The rejection of claims 1, 3, 4 and 12 under 35 U.S.C. §102(b) as being anticipated by Uchida '304 (hereinafter Uchida) has been obviated by appropriate amendment and should be withdrawn.

IEEE Std 1149.1-1990 describes an identification register that can capture a single vendor defined identification code and a **supplemental** identification code in response to an IDCODE instruction or a USERCODE instruction, respectively (see section 11.1 of the IEEE Std 1149.1-1990). IEEE Std 1149.1-1990 does not appear to disclose or suggest a circuit configured to generate **a plurality of identification codes** in response to one or more voltage levels on one or more inputs **and** a package comprising one or more pins dedicated to providing the one or more voltage levels to respective ones of the one or more inputs, where the one or more voltage levels determine which of the plurality of identification codes is generated by the circuit, as presently claimed. Therefore, IEEE Std 1149.1-1990 does not disclose or suggest each and every element of the presently claimed invention, arranged as in the claims. As such, the presently claimed invention is fully patentable over IEEE Std 1149.1-1990 and the rejection should be withdrawn.

Uchida is directed to a semiconductor integrated circuit (Title). Uchida describes selecting an identification code for a device via bond optioning bonding pads to a GND pin during assembly (see column 3, line 58 through column 4, line 5 and column 6, lines

14-33 of Uchida). Uchida does not disclose or suggest a package comprising one or more pins dedicated to providing one or more voltage levels to respective ones of one or more inputs, where the one or more voltage levels determine which of the plurality of identification codes is generated by the circuit, as presently claimed. Therefore, Uchida does not disclose or suggest each and every element of the presently claimed invention, arranged as in the present claims. As such, the presently claimed invention is fully patentable over Uchida and the rejection should be withdrawn.

In contrast to IEEE Std 1149.1-1990 and Uchida, the presently claimed invention (claim 1) provides (i) a circuit configured to generate a plurality of identification codes in response to one or more voltage levels on one or more inputs and (ii) a package comprising one or more pins dedicated to providing the one or more voltage levels to respective ones of the one or more inputs, where the one or more voltage levels determine which of the plurality of identification codes is generated by the circuit. Claims 16 and 20 include similar recitations. Neither IEEE Std 1149.1-1990 nor Uchida disclose or suggest each and every element of the presently claimed invention, arranged as in the claims. As such, the presently claimed invention is fully patentable over both IEEE Std 1149.1-1990 and Uchida and the rejections should be withdrawn.

Claims 2-10, and 12 depend, either directly or indirectly, from claim 1 which is believed to be allowable. As such, claims 2-10, and 12 are fully patentable over IEEE Std 1149.1-1990 and Uchida and the rejections should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 16, 18, and 19 under 35 U.S.C. §103(a) as being obvious over "IEEE Standard Test Access Port and Boundary-Scan Architecture, IEEE Std 1149.1-1990" (hereinafter IEEE Std 1149.1-1990) in view of the "Supplement to IEEE Std 1149.1-1990, IEEE Standard Test Access Port and Boundary-Scan Architecture" (hereinafter Supplement) has been obviated by appropriate amendment and should be withdrawn.

The rejection of claim 11 under 35 U.S.C. §103(a) as being obvious over IEEE Std. 1149.1-1990 in view of Carmichael et al. '311 (hereinafter Carmichael) has been obviated by appropriate amendment and should be withdrawn.

The rejection of claims 13 and 14 under 35 U.S.C. §103(a) as being obvious over Uchida in view of Carmichael has been obviated by appropriate amendment and should be withdrawn.

The rejection of claim 15 under 35 U.S.C. §103(a) as being obvious over Uchida in view of Carmichael, and in further view of Wegner et al. '246 (hereinafter Wegner) has been obviated by appropriate amendment and should be withdrawn.

The rejection of claim 16 under 35 U.S.C. §103(a) as being obvious over the "Background of the Invention" section of the present specification (hereinafter Background) in view of Supplement has been obviated by appropriate amendment and should be withdrawn.

The rejection of claim 17 under 35 U.S.C. §103(a) as being obvious over Background in view of Supplement, and in further view of IBM TDB Publication "Using a portion of the boundary register as the identification register" (hereinafter IBM) has been obviated by appropriate amendment and should be withdrawn.

IEEE Std 1149.1-1990 describes a test access port that can provide access to many test support functions built into a component (see section 3 of IEEE Standard 1149.1-1990). The test access port can capture an identification code of the component (see section 11 of the IEEE Standard 1149.1-1990). IEEE Std 1149.1-1990 appears silent regarding (i) dedicating one or more pins of a package to selecting any of a plurality of identification codes, (ii) generating the plurality of identification codes in response to voltage levels on the one or more dedicated pins and (iii) providing an indication of the voltage levels to be applied to each of the one or more dedicated pins, as presently claimed.

Background describes a test access port and an ID code register of an IEEE Std. 1149.1-1990 compliant device. Background is silent regarding (i) dedicating one or more pins of a package to

selecting any of a plurality of identification codes, (ii) generating the plurality of identification codes in response to voltage levels on the one or more dedicated pins and (iii) providing an indication of the voltage levels to be applied to each of the one or more dedicated pins, as presently claimed.

Supplement provides a hardware description language to describe components that conform to IEEE Standard 1149.1-1990 (Abstract of the Supplement). Supplement does not appear to cure the deficiencies of either IEEE Std 1149.1-1990 or Background. Specifically, Supplement also appears silent regarding (i) dedicating one or more pins of a package to selecting any of a plurality of identification codes, (ii) generating the plurality of identification codes in response to voltage levels on the one or more dedicated pins and (iii) providing an indication of the voltage levels to be applied to each of the one or more dedicated pins, as presently claimed.

In contrast, the presently pending claim 16 provides the steps of (i) dedicating one or more pins of a package to selecting any of a plurality of identification codes, (ii) generating the plurality of identification codes in response to voltage levels on the one or more pins and (iii) providing an indication of the voltage levels to be applied to each of the one or more pins. Neither the combination of IEEE Standard 1149.1-1990 and Supplement nor the combination of Background and Supplement teach or suggest

each and every element of the presently claimed invention. As such, the presently pending claim 16 is fully patentable over the cited references and the rejection should be withdrawn.

Claims 17, 18 and 19 depend, either directly or indirectly, from claim 16 which is believed to be allowable. As such, claims 17, 18 and 19 are believed to be fully patentable over the cited references and the rejection should be withdrawn.

Claims 11, and 13-15 depend, either directly or indirectly, from claim 1 which is believed to be allowable. As such, claims 11 and 13-15 are believed to be fully patentable over the cited references and the rejections should be withdrawn.

New claims 21-25 depend, either directly or indirectly, from claims 1 and 16 which are believed to be allowable. As such, the presently claimed invention is fully patentable over the cited references and the rejections should be withdrawn.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge our office Account No. 50-0541.

Respectfully submitted,

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